Claims 1-10 (cancelled).

11. (currently amended): A method comprising:

querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit by comparing an address of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included; and

communicating the indication to an operating system being executed on the processor unit.

12. (cancelled).

13. (original): A method as described in claim 11, further comprising establishing a relative amount of time to access the set of data by the processor unit based on the indication which indicates whether the set of data resides in the cache memory.

14. (original): A method as described in claim 11, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

15. (original): A method as described in claim 11, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

16. (original): A method as described in claim 11, wherein the querying and the receiving are performed without reading the set of data from the cache memory to the processor unit and without writing the set of data from the processor unit to the cache memory.

17. (cancelled): A method as described in claim 11, further comprising:

comparing an address of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

providing, based on the comparing, an indication to the processor unit of whether the address of the set of data is included in the cache memory, wherein if

the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included.

18. (original): One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 11.

19. (previously presented): A method comprising:

comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;

providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;

establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included; and

communicating the indication, by the processor unit, to software being executed on the processor unit.

20. (cancelled).

21. (original): A method as described in claim 19, wherein the software is selected from the group consisting of an operating system and an application.

22. (original): A method as described in claim 19, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

23. (original): One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 19.

Claims 24-41 (cancelled).

42. (currently amended): For use on a processor unit that is communicatively coupled to a comparison unit that is communicatively coupled to a cache memory, a cache residency test instruction, which when executed on the processor unit, configures the comparison unit to perform acts comprising:

comparing an address received from the processor unit with an address in the cache memory;

providing an indication to the processor unit based on the comparing of whether the address is included in the cache memory, wherein the indication indicates to the processor unit whether the address is included in the cache memory, and if so, at which level of a plurality of levels of the cache memory the address is included; and

communicating the indication to an operating system being executed by the processor unit.

43. (cancelled).

44. (original): A cache residency test instruction as described in claim 42, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

45. (currently amended): A system comprising:

a cache memory that includes a plurality of levels; and

a processor unit communicatively coupled to the cache memory, wherein

the processor unit includes a cache residency test instruction that, when executed, configures the processor unit:

to query whether a set of data resides in the cache memory;

to receive an indication from the query of whether the set of data resides in the cache memory, wherein if the set of data is included in the cache memory, the indication indicates at which level of the plurality of levels the set of data is included;

to establish a relative amount of time to access the set of data; and

to communicate the indication and the relative amount of time to software being executed on the processor unit.

46. (original): A system as described in claim 45, further comprising a comparison unit, wherein execution of the cache residency test instruction by the processor unit configures the comparison unit to compare an address of the set of data with at least one other address of the cache memory in response to the query.

47. (cancelled).

48. (original): A system as described in claim 45, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

49. (original): A system as described in claim 45, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

Claims 50-55 (cancelled).

56. (currently amended): A processor chip comprising

a processor unit having a coupling for communicatively coupling the processor unit to a cache memory having a plurality of levels, wherein:

the processor unit includes storage for a cache residency test instruction; and

an execution of the cache residency test instruction with the processor unit configures the processor unit to determine if a set of data resides in the cache memory, and if so, establish which of the plurality of levels the set of data resides, establish a relative amount of time to access the set of data, and communicate a result of the determination and the relative amount of time to software being executed on the processor unit.

57. (original): A processor chip as described in claim 56, further comprising a second processor unit having:

a coupling for communicatively coupled the second processor unit to the cache memory;

storage for a second cache residency test instruction; and

an execution of the second cache residency test instruction with the second processor unit configures the second processor unit to determine if a set of data resides in the cache memory and communicate a result of the determination to software being executed on the second processor unit.

58. (original): A processor chip as described in claim 56, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

59. (original): A processor chip as described in claim 56, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

60. (original): A processor chip as described in claim 56, wherein the cache memory is selected from the group consisting of:

a cache memory located on the processor chip;

a cache memory located off the processor chip; and

a combination of the forgoing.

61. (original): A processor chip as described in claim 56, wherein the cache memory is configured as a semiconductor-based memory.

62. (original): A processor chip as described in claim 56, wherein the software is selected from the group consisting of an operating system and an application.

63. (currently amended): A computing device comprising:

a storage device; and

a processor chip, communicatively coupled to the storage device, and including:

a cache memory having a plurality of levels; and

a processor unit communicatively coupled to the cache memory, wherein the processor unit includes storage for a cache residency test

instruction that, when executed by the processor unit, configures the processor unit to determine if a set of data resides in the cache memory, and if so, which of the plurality of levels of the cache memory the set of data resides, and to communicate a result of the determination to an operating system being executed on the processor chip.

64. (previously presented): A computing device as described in claim 63, wherein the processor chip further comprises a second processor unit communicatively coupled to the cache memory, wherein the second processor unit includes storage for a second cache residency test instruction that, when executed by the second processor unit, configures the second processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to the operating system being executed on the processor chip

65. (original): A computing device as described in claim 63, wherein the set of data is selected from the group consisting of:
an instruction for controlling the processor unit; and
data for being processed by the processor unit.

66. (original): A computing device as described in claim 63, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

67. (original): A computing device as described in claim 63, wherein the cache memory is configured as a semiconductor-based memory.

68. (cancelled).